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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/495,813	02/01/2000	Gregory Allen North	2836-P100US	5319
31127	7590	11/07/2005	EXAMINER	
JAMES J. MURPHY THOMPSON AND KNIGHT LLP 1700 PACIFIC AVENUE SUITE 3300 DALLAS, TX 75201			FERRIS III, FRED O	
			ART UNIT	PAPER NUMBER
			2128	

DATE MAILED: 11/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/495,813

Applicant(s)

NORTH ET AL.

Examiner

Fred Ferris

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 6 September 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-65 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-65 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 February 2000 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. *This Supplemental Office Action supercedes the previous office action of 25 February 2004 that was responsive to an improperly entered amendment canceling claims 1-50 and 57-65. Claims 1-65 as filed 1 February 2000 currently remain pending in this application. The period for reply is hereby restarted in accordance with MPEP 710.06. Claims 1-65 now stand rejected by the examiner.*

Drawings

2. *This application has been filed with informal drawings that are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings.*

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. ***Claims 16-43 are rejected under 35 U.S.C. 101 because the claimed invention is drawn to non-statutory subject matter.***

Per independent claims 16, 26, 33 and 39: The Examiner submits that method of claims 16, 26, 33 and 39, as written, are merely drawn to a mental process method since the language of the claims can be interpreted as meaning the method is carried out by a mental process augmented (calculated) using pencil and paper. (i.e. not a machine or computer process) See Figure

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MPEP 2111 [R-1] recites the following:

***"2111 [R-1] Claim Interpretation; Broadest Reasonable Interpretation
CLAIMS MUST BE GIVEN THEIR BROADEST REASONABLE
INTERPRETATION***

During patent examination, the pending claims must be "given their broadest reasonable interpretation consistent with the specification." In re Hyatt, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000).< Applicant always has the opportunity to amend the claims during prosecution, and broad interpretation by the examiner reduces the possibility that the claim, once issued, will be interpreted more broadly than is justified. In re Prater, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969) (Claim 9 was directed to a process of analyzing data generated by mass spectrographic analysis of a gas. The process comprised selecting the data to be analyzed by subjecting the data to a mathematical manipulation. The examiner made rejections under 35 U.S.C. 101 and 102. In the 35 U.S.C. 102 rejection, the examiner explained that the claim was anticipated by a mental process augmented by pencil and paper markings. The court agreed that the claim was not limited to using a machine to carry out the process since the claim did not explicitly set forth the machine. The court explained that "reading a claim in light of the specification, to thereby interpret limitations explicitly recited in the claim, is a quite different thing from reading limitations of the specification into a claim, to thereby narrow the scope of the claim by implicitly adding disclosed limitations which have no express basis in the claim." The court found that applicant was advocating the latter, i.e., the impermissible importation of subject matter from the specification into the claim.). See also In re Morris, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997) (The court held that the PTO is not required, in the course of prosecution, to interpret claims in applications in the same manner as a court would interpret claims in an infringement suit. Rather, the "PTO applies to verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in applicant's specification.")"

The Examiner further submits that, in view of the language of the claims, Applicant's have merely claimed a method for manipulation of abstract ideas by a mental process and have not specifically set forth a machine or computer process for performing the actual secure operation, preventing access, and synthesizing/emulating translation tables, as recited in independent claims 16, 26, 33 and 39. Dependent claims inherit the defects of the claims from which they depend.

Double Patenting

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

4. Claims 26-32 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-7 of prior U.S. Patent No. 6,754,784 issued to North et al. This is a double patenting rejection.

In this case claims 26-32 of the present invention are identical in verse and claim the same invention as claims 1-7 of U.S. Patent No. 6,754,784.

5. Claims 51-56 are provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 51-56 of copending Application No. 09/496,813. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

In this case claims 51-56 of the present invention are identical in verse and claim the same invention as claims 51-56 of U.S. Patent Application No. 09/496,813.

Claim Rejections - 35 USC § 112

6. Claims 1-25, and 44-50 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Specifically, Independent claims 1, 16, and 44 recite a system on a chip that is not described by the specification sufficiently to allow a skilled artisan to make and/or use the invention without undue experimentation. The specification and Figures 1-2 depict a multi-chip design based on the ARM720T including an APB bus and bridge network between the processor and support components and therefore do not disclose a system on chip (SoC) design in accordance with the claims. Dependent claims 2-15, 17-25, and 45-50 inherit this defect.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 33-43 and 57-65 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by U.S. Patent 6,446,034 issued to Egolf.

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Regarding independent claims 33, 39, and 57: Egolf discloses generating virtual translation tables for creating physical addresses to a memory space using registers to access information on memory spaces, virtual addresses, and pointers to information for controlling memory access. For example, at column 13, line 63 Egolf recites:

"where the virtual address structure is modified utilizing standard instructions that typically do not have side effects. In the preferred embodiment, this is addressed by "coloring" memory containing virtual memory translation tables. By "color" is meant that the emulator marks memory in a special way so that updates to that memory by the emulated system can be noted and special action taken. In the case here, the special action is that the PT pointer valid flag 330 for all of the segment descriptor registers are cleared whenever any of the higher level virtual memory translation tables are modified. Note that it is unnecessary to clear the PT pointer valid flag 330 when page table entries 214 in page tables 212 are modified since the PT pointers 320 access the virtual memory hierarchy at this level."

Figures 2-14 and Tables T-1 to T-7 of Egolf further disclose accessing table descriptors, comparing indices, pointers to translation tables, indexing registers, and entity storage. (Abstract, Summary of Invention, CL6-L1-44, CL8-L12-65, CL10-L10-62)

Regarding dependent claims 34-38, 40-43, 58-65, and 67-69: This group of claims merely addresses limitations relating to memory (level) access control, cache access, and buffering which is taught by Engolf as cited above.

8. Claims 33-43 and 57-65 are also rejected under 35 U.S.C. 102(b) as being clearly anticipated by U.S. Patent 6,003,123 (of record) issued to Carter et al.

Regarding independent claims 33, 39, and 57: Carter et al discloses techniques for memory access control incorporating translation tables for creating physical addresses to a memory space, registers to access information on memory spaces, virtual addresses, pointers to information for controlling memory access, accessing table descriptors, comparing indices, pointers to translation tables, indexing registers,

and entity storage that are functionally equivalent to the claimed invention. For example, at column 13, line 63 Carter recites:

"In accordance with one aspect of the invention, a data processing system comprises shared memory for storing instructions and data for plural programs, the shared memory being accessed in response to pointers. Guarded pointers address memory locations to which access is restricted. Each guarded pointer is a processor word which fully identifies a protected segment in memory and an address within the protected segment. Processor hardware distinguishes guarded pointers from other words and is operable under program control to modify guarded pointers. Modification of guarded pointers is restricted so that only addresses within the identified segment can be created. Thus, access outside of a protected segment is prevented. A permission field in the guarded pointer indicates permissible access to the identified memory segment such as read only or read/write. By providing the full virtual address, segment information, and a permission field, segment checks and permission checks can be performed during a memory access without requiring additional machine cycles."

Regarding dependent claims 34-38, 40-43, and 58-65: This group of claims merely addresses limitations relating to memory (level) access control, cache access, and buffering which is taught by Carter as cited above. Also see: Abstract, Summary of Invention, CL4-L40-65, CL9-L23-48, CL10-L24-67, CL15-L40-CL18-L8, Figs. 1-6, 9-10, 16-16)

9. Claims 44-50, and 51-56 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by U.S. Patent 5,914,941 issued to Janky.

Per independent claims 44 and 51: Janky discloses a personal (hand-held) audio decoder device containing a CPU capable of decoding a stream of digital audio data to generate analog audio. The unit disclosed by Janky also includes memory for instructions, a DAC for generating audio, a security (encryption) circuit, programmable elements (ROM/FLASH), security procedure in memory, and secure modes. (Abstract, Summary of Invention, CL7-L18-52, CL8-L34-65, CL9-L25-55, CL11-L30, 46, Figs. 2-5)

Per dependent claims 45-49, and 52-56: As cited above, Janky includes programmable elements (fuses), ROM memory, a microprocessor, security circuit, and encrypted (locked) entries. Further, compatibility with standard digital audio data formats such as MS audio, ACC, and MPEGx, layer 3 encoded data, and would be inherent in Janky or nearly any portable audio decoder.

10. Independent claims 1, 44, and 51 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by U.S. Patent 6,421,305 issued to Gioscia et al.

Per claim 51: Gioscia discloses personal (hand-held) audio decoder device containing a CPU capable of decoding a stream of digital audio data to generate analog audio and includes memory for instructions and a DAC for generating audio. (Abstract, Summary of Invention, CL4-L35-CL5-L45, Figs 1-3)

11. Claims 44-50, and 51-56 are further rejected under 35 U.S.C. 102(b) as being clearly anticipated by U.S. Patent 6,629,000 issued to Moon et al.

Per claims 44-50 and 51-56: Moon discloses portable personal audio decoder device containing a CPU capable of decoding a stream of digital audio data to generate analog audio and includes memory for instructions and a DAC for generating audio from various digital formats including MPEG. (Abstract, Summary of Invention, CL3-L35-65, CL4-L19-65, CL5-L19-CL6-L35, Figs 1-3f)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. Claims 1-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,467,009 issue to Winegarden et al in view of US Patent 5,892,900 issued to Ginter et al

Regarding independent claims 1 and 16: Winegarden teaches a system on chip (SoC) inclusive of a CPU operating in response to instructions (Figs. 1, 2, 22), and interface with access to circuitry (external), programmable elements, JTAG port, and non-volatile memory with security features (CL34-L50-CL35-L10, CL35-L33-61, Fig. 2, 32-42).

Winegarden does not explicitly disclose executing security code and controlling access.

Ginter et al discloses determining whether a security procedure (col 76 ln 51-64) is called for during system initialization from boot memory (col 76 ln 51-64 and col 73 ln 56-65); and attempting to execute a selected security procedure when a security procedure is called for during system initialization (col 74 ln 10-55 and col 76 ln 51-64), comprising the steps of: mapping a vector to the selected location in boot memory storing security code calling a selected security procedure (col 76 ln 51-64, Ginter et al discloses vector based processing means (col 1 ln 26-63). Mapping a vector to a selected location for execution of computer code is inherent to any execution means to execute program code in memory of a vector based processing system; and operating the system in a secure environment in response to the called security procedure (col 51 ln 51-64). Ginter et al discloses loading of services during system boot including executing the service code (i.e. security) in boot memory to determine whether the called service is valid (col 100 ln 41-45) and operating the service if the service is valid (col 100 ln 42-45). Services of Ginter et al's teaching comprises program code, which operates functions for that service (service module 100 ln 35-45). One of ordinary skill in the art at the time of the applicant's invention would have been able to further modify Ginter's teachings to validate the security procedure by executing the security code in boot memory. This have been obvious since it would have enhanced security by validating a proper procedure being loaded correctly. Ginter et al further discloses disabling debug circuitry forming a part of the system on a chip to (col 78 ln 56-66) at power-on reset (col 76 ln 51-64 and col 78 ln 41-66), to prevent access by an unauthorized party to security resources (col 78 ln 56-66).

Per claims 2-4: Winegarden teaches a system inclusive of a JTAG port, interface port for emulation, and external devices (CL3-L43-65, Fig. 2).

Per claims 5-8 and 20-25: Ginter et al discloses searching for the called security procedure in external memory coupled to the system on a chip (col 76 ln 51-64). Ginter et al discloses executing boot code (col 76 ln 51-col 77 ln 9). Ginter et al does not explicitly teach executing default boot code when a security procedure is invalid. The office take official notice to the step of executing a default boot code when a program is invalid is well known in the art, for booting systems in a safe mode to correct any problems. A security procedure consists of program code. It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Ginter et al to execute default boot code when a security procedure is invalid because it would have increased usability by allowing the user to debug any errors found in the system. Ginter et al further discloses the sub step of reading the state of a set of programmable elements (external control signal, col 76 ln 50-64, switch, col 74 ln 29-64 and col 78 ln 41-55). Ginter et al further discloses the sub step of reading being performed by logic gates (AND gate, col 76 ln 51-64). Ginter et al discloses the sub step of reading being performed by logic gates (AND gate, col 76 ln 51-64).

Per claims 9-15: Winegarden teaches a system inclusive of fused programmable elements, read-only cells, write-only cells, and flash memory (sections 5.1-5.3, Figs. 1-32)

13. Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable in further view of US Patent 6,519,721 issued to Gorman.

Regarding claims 17-19: Ginter et al discloses of booting for unsecured operation if a security procedure is not called for in response to said step of determining (col 76 ln 38-64) and the elements of independent claim 1 and 16 as noted above

Winegarden and Ginter do not explicitly teach enabling debug circuitry. Gorman discloses program loading through disabling and enabling debug circuitry (col 2 ln 3 ln 64 -col 4 ln 23). Both Ginter et al and Gorman disclose methods of loading executing program code. It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to combine the teachings of Gorman et al within the system of Ginter et al because it would have increased security by preventing access to program's operation (see Gorman, col 1 ln 46-60) as well as provide debug circuitry after boot up. Ginter et al further discloses internal and external memory (col 71 ln 16- col 72 ln 55) and booting the system from internal or external memory (col 76 ln 56-64) by selecting one of internal AND external boot memory options (executing instruction from an address in SPU memory... or otherwise external to the CPU/SPU, col 76 ln 51-64). The steps of in response to selection of the internal boot memory option mapping the vector to a default location in internal boot memory is inherent to the execution means of executing existing instructions from an address in SPU memory (col 76 ln 51-64). The step of in response to the selection of the external boot memory option, mapping the vector to a location in external boot memory and executing boot code pointed-to by the

vector is inherent to the execution means of executing instructions from main memory or otherwise external to the CPU/SPU (col 76 ln 51-64). Ginter et al further discloses internal and external memory (col 71 ln 16-col 72 ln 55) and booting the system from internal or external memory (col 76 ln 56-64). The step of remapping a chip select signal controlling the external memory to point-to currently executing memory space and changing a program counter to the vector such that a fetch of an instruction changing the program counter is completed prior to completion of said step of remapping is inherent to the execution of instruction from external memory (col 76 ln 56-64) of a vector based processing system. Ginter et al further discloses a power on reset of the system (col 76 ln 51-53). A CPU reset vector is inherent to the resetting of the system in order to instruct the system during a power-on reset.

13. Claims 33-43 and 57-69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patent 5,724,551 issued to Greenstein et al in view of EP 0 656 592 A1 (of record) issued to Revilla.

Independent claim 33 is drawn to:

Method of synthesizing translation tables by:

Setting up register storing access info to memory spaces

Generating virtual addresses, pointer to info in register controlling access to memory

Accessing selected info at pointer from register

Generating physical address to memory space from info in register

Regarding independent claim 33 and 66: Greenstein et al discloses generating (synthesizing) translation tables in controlling memory access by storing memory space access information, generating virtual addresses, accessing selected memory space

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information (entries, descriptors, etc.), registers controlling memory access, and generating physical addresses into the memory space. (Abstract, Summary of Invention, CL8-L27-49, 64-67, CL9-L12-3, CL11-L14 to CL9-L55, CL15-L23-35, Figs. 1-3, 5-7, 9-23)

Greenstein does not explicitly disclose the use of a translation register in controlling memory access.

Revilla teaches memory (level) access control where address translation is performed via a first and second translation register, by controlling cache access, and using table-walks. (Abstract, Summary of Invention, CL4-L12-55, CL6-L12-45, CL7-L20 to CL8-L33, Figs. 2-5)

It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teachings of Greenstein relating to generating (synthesizing) translation tables in controlling memory access by storing memory space access information, with the teachings of Revilla relating to memory access control where address translation is performed via a first and second translation register, cache access, and using table-walks, to realize the claimed invention. It would also have been obvious to point to the translation register with a base pointer as this is a common technique used in the art when accessing data tables.

An obvious motivation exists since this area of technology is highly competitive with many techniques for access control (privatization) available in the market place and large amounts of money being spent in product development and improvement.

Accordingly, a skilled artisan would have made an effort to become aware of what

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capabilities had already been developed in the market place and, hence, would have been motivated to modify the teachings of Greenstein with the teachings of Revilla in order to reduce development time and cost.

Independent claim 39 is drawn to:

Method of emulated translation table by:

Emulating translation register with entries and descriptors

Emulating index register, storing entity index, with translation register

Pointing to translation register with base pointer

Generating address and index bits to register

Comparing index bits form address with index indices

Selectively accessing table descriptor after comparing

Regarding independent claims 39 and 57: As previously cited, Greenstein et al discloses generating (synthesizing) translation tables in controlling memory access by storing memory space access information, generating virtual addresses, accessing selected memory space information (entries, descriptors, etc.), registers controlling memory access, and generating physical addresses into the memory space. (Abstract, Summary of Invention, CL8-L27-49, 64-67, CL9-L12-3, CL11-L14 to CL9-L55, CL15-L23-35, Figs. 1-3, 5-7, 9-23) Greenstein also discloses address and table indexing by register (CL15-L27, Fig. 7).

Greenstein does not explicitly disclose the use of a translation register in controlling memory access.

Revilla teaches memory (level) access control where address translation is performed via a first and second translation register, by controlling cache access, and using table-walks. (Abstract, Summary of Invention, CL4-L12-55, CL6-L12-45, CL7-L20

to CL8-L33, Figs. 2-5) Revilla further discloses comparing register bits (indexing) to generate (form) physical and virtual addresses (CL5-L20-45, Figs. 2-5)

It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teachings of Greenstein relating to generating (synthesizing) translation tables in controlling memory access by storing memory space access information, with the teachings of Revilla relating to memory access control where address translation is performed via a first and second translation register, cache access, and using table-walks, to realize the claimed invention. It would also have been obvious to point to the translation register with a base pointer as this is a common technique used in the art when accessing data tables.

An obvious motivation exists since this area of technology is highly competitive with many techniques for access control (privatization) available in the market place and large amounts of money being spent in product development and improvement. Accordingly, a skilled artisan would have made an effort to become aware of what capabilities had already been developed in the market place and, hence, would have been motivated to modify the teachings of Greenstein with the teachings of Revilla in order to reduce development time and cost.

Regarding dependent claims 34-38, 40-43, 58-65, and 67-69: This group of claims merely addresses limitations relating to memory (level) access control, cache access, and buffering which is taught by Greenstein and Revilla as previously cited above.

14. Claims 51-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,629,000 issued to Moon et al in view of U.S. Patent 5,867,579 issued to Saito.

Independent claim 51 is drawn to:
Audio decoder comprising:
CPU decoding stream of digital audio data
Memory for instructions
DAC for generating audio

Per claims 51-56: Moon discloses a portable personal audio decoder device containing a CPU capable of decoding a stream of digital audio data to generate analog audio and further includes memory for instructions, a DAC for generating audio from various digital formats (including MPEG), and programmable (ROM/FLASH) elements. (Abstract, Summary of Invention, CL3-L35-65, CL4-L19-65, CL5-L19-CL6-L35, Figs 1-3f)

Moon does not explicitly disclose a security (encryption) circuit for secure operation.

Saito teaches the use of a memory based encryption (security) circuit incorporating restricted access programmable elements (ROM/EEPROM) and a memory for storing executable encryption (security) procedure. (Abstract, Summary of Invention, CL11-L21-CL12-L45, CL13-L45-CL14-L50, CL16-L15-61, CL19-L61-CL20-L25, Figs. 4, 5, 9-12)

It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teachings of Moon relating to a portable personal audio decoder containing a CPU capable of decoding a stream of digital audio

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data to generate analog audio, with the teachings of Saito relating to the use of a memory based encryption (security) circuit incorporating restricted access programmable elements, to realize the claimed invention. It would further have been obvious to only allow the security circuit access to programmable elements for initiating a secure mode in order to keep the security circuit from being defeated. An obvious motivation exists since this area of technology is highly competitive with many portable digital audio devices available in the market place, and large amounts of money being spent in product development and improvement. (See Saito Abstract, for example) Accordingly, a skilled artisan would have made an effort to become aware of what capabilities had already been developed in the market place and, hence, would have been motivated to modify the teachings of Moon with the teachings of either Saito in order to reduce development time and cost.

Conclusion

15. *The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.*

U.S. Patent 6,385,596 issued to Wiser teaches secure music distribution.

U.S. Patent Publication 2002/0094084 A1 teaches conditional access.

U.S. Patent 5,978,689 teaches personal audio system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 571-272-3778 and whose normal working hours are 8:30am to 5:00pm Monday to Friday. Any inquiry

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of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 571-272-3700. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached at 571-272-3780. The Official Fax Number is: (703) 872-9306

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October 20, 2005

